by the value of the external capacitor or output voltage. For example, if the external capacitor is altered, the current required for the switching regulator to enter or exit the low power mode will be changed. Furthermore, in conventional switching regulators, if the voltage of the input driver changes, the point that the switching regulator enters or exits low power mode will change.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A switching regulator, comprising:

a driver coupled to receive a first high side control signal [reference voltage];

an input switching device having a source node, a drain node, and a control node, the control node coupled to an output of the driver, the drain node coupled to receive an input voltage;

a diode coupled between the source node of the input switching device and ground;

an inductor having a first end coupled to the source node of the input switching device;

a first output switching device having a drain node coupled to the second end of the inductor, the first output switching device having a control node coupled to a second high side control signal [output];

a second output switching device having a drain node coupled to the second end of the inductor, the [first]

second output switching device having a control node coupled to a low side control signal [output], the second output switching device having a source node coupled to ground;

an output load coupled [to] between the source nodes of the first and second output switching devices;

an output capacitor coupled between the source nodes of the first and second output switching devices to provide an output voltage; and

a low power control circuit coupled across the inductor, wherein the low power control circuit monitors the current [across] delivered to the output load and automatically initiates the low power mode of the switching regulator independent of the value of the output voltage, the output capacitor, the inductor [load] and the input voltage.

2. (currently amended) A switching regulator as recited in claim 1, wherein the low power control circuit comprises:

a low power switching device having a control node coupled to receive the high side control signal [output] and a drain node coupled to the second end of the inductor;

an amplifier coupled to the source node of the low power switching device and the first output switching device;

a first current mirror coupled to the amplifier to mirror [the difference between] the output current delivered to [through] the output load [and the current supplied at the second end of the inductor] through the low power switching device;

a second current mirror coupled to the first current mirror;

a current source coupled between [to] the second current mirror and ground;

a capacitor coupled across the current source;

a comparator coupled to the second current mirror and coupled to receive a predetermined voltage source to compare the voltage across the capacitor with the predetermined voltage source;

a first AND gate coupled to the comparator and to receive the low power mode signal;

an inverter coupled to receive the low power mode signal to generate an inverted low power mode signal;

a second AND gate coupled to the comparator and to receive the inverted low power mode signal and the inductive switch signal;

a first counter, having an input and an output, the input coupled to the first AND gate to provide a low power entry signal at the output, the output coupled to the second AND gate; and

a second counter, having an input and an output, the input coupled to the second AND gate to provide a low power exit signal at the output, the output coupled to the first AND gate.

3. (original) The switching regulator as recited in claim 1, wherein the first input switching device is a transistor.

4. (original) The switching regulator as recited in claim 1, wherein the second input switching device is a transistor.

5. (original) The switching regulator as recited in claim 1, wherein the first output switching device is a transistor.

6. (original) The switching regulator as recited in claim 1, wherein the second output switching device is a transistor.

7. (original) The switching regulator as recited in claim 1, wherein the first input switching device is a metal-oxide-semiconductor field-effect transistor (Mos FET).

8. (original) The switching regulator as recited in claim 1, wherein the second input switching device is a Mos FET transistor.

9. (original) The switching regulator as recited in claim 1, wherein the first output switching device is a Mos FET transistor.

10. (original) The switching regulator as recited in claim 1, wherein the second output switching device is a Mos FET transistor.

11. (currently amended) The switching regulator as recited in claim 1, wherein the output load [comprises:
a capacitor; and] is
a resistor [coupled in parallel with the capacitor].

12. (original) The switching regulator as recited in claim 2, wherein the low power switching device is a transistor.

13. (original) The switching regulator as recited in claim 2, wherein the low power switching device is a sense FET transistor.

14. (currently amended) The switching regulator as recited in claim 2, wherein the first current mirror, comprises:

a first transistor, having a drain node coupled to the source node of the low power switching device; and

a second transistor coupled to the first transistor, the control node of the first and second transistors coupled to the amplifier, the source node of the second transistor coupled to the source node of the first transistor.

1[3]5. (currently amended) The switching regulator as recited in claim 2, wherein the second current mirror, comprises:

a first transistor, having a drain node, a source node, and a control node, the drain node coupled to the control node and the drain node coupled to the first current mirror; and

a second transistor having a drain node, a control node and a source node, the control node coupled to the control node of the first transistor, the source node coupled to the source node of the first transistor, the drain node coupled to the capacitor.